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⑭録音機能付ヘッドホーン

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明　細　書

1. 発明の名称

録音機能付ヘッドホーン

2. 特許請求の範囲

(1) 音声を出力する電子機器に使用するヘッドホーンにおいて、録音・再生用スイッチ、音声の入出力に関する制御手段、ADまたは手段、半導体メモリ、記憶手段、入力端子を有し、入力端子から入力される音声信号の一部を、スイッチ操作により録音・再生できるというIC録音機能を備えたことを特徴とする録音機能付ヘッドホーン。

(2) 繰り返し再生する手段を有することを特徴とした、特許請求の範囲第1項記載の録音機能付ヘッドホーン。

(3) 自分の声を入力するためのマイクを有することを特徴とした、特許請求の範囲第1項記載の録音機能付ヘッドホーン。

3. 発明の詳細な説明

本発明はメモリーによる録音機能を有する、ヘッドホーンに関するものである。

近年、エレクトロニクスの発達によりテレビ・ラジカセ・ステレオ等の音声を出力する電子機器はめまぐるしい発展をとげ、多種多用の製品が市場に出回っている。それに伴い、音声を出力する媒体も一般的なスピーカから、個人で楽しむイヤホーン・ヘッドホーンまで、それぞれの使用方法に応じた媒体が用意されている。しかし、これらはあくまでも入力された信号を音声に変換して出力しているだけであり、英語のレッスンのように、同じ所を繰り返して聞く場合には、録音媒体である磁気テープ等を操作して繰り返し再生するため、操作がめんどうである上、時間がかかる。そこで、本発明はこのような不具合をなくし、短時間に繰り返して再生することを可能にし、軽量化を計るためのものであり、以下図を使って説明する。

第1図は、本発明実施例の録音機能付ヘッドホーンの回路構成図である。

本発明の録音機能付ヘッドホーンを使用する場合、まず、自分が録音したいと思う時に録音用スイッチ3を操作する。この信号は、スイッチ制御回路4を介して、制御回路5に与えられる。この状態でマイク15または入力端子16より音声アナログ信号が入力されると、入力アンプ14、入力フィルタ13を通して、ADM符号化回路により、デジタル化される。これが、アドレス回路6の情報により、メモリ部7に書き込まれることにより、音声が録音される。

次に、録音した音声を再生する場合には、再生用スイッチ1を操作する。この信号は、スイッチ制御回路2を介して、制御回路5に与えられる。そうすると、制御回路5は、アドレス回路6の情報により、必要な音声をメモリ部7より取り出しADM復号化回路によってアナログ化する。この音声は、出力フィルタ9、出力アンプ10を介してスピーカ11に伝わり、音声として出力される。

尚、第2図に全体のシステムを略記する。音響機器20はテープレコーダ、ラジオ等の出力手段であり、ヘッドホーン21が取付けられる。ヘッドホーン21の中はスピーカー22とIO録音機構23とから構成される。このように、メモリを使って録音・再生を行なえば、スイッチ操作が容易になり、また、短時間で録音した音声を再生することができるため、従来のように、録音したテープ等の媒体を操作する必要がなく、また、テープ録音等よりは、かなり経済化されるため、教育用等には特に効果は大きい。尚、本実施例はただ再生するだけとして記述したが、繰り返し再生する手段を有していれば、短時間に同じ音声を何度でも聞くことができ、また自分の声を入出するマイクを有していれば、自分の声と入力端子から入力された音声との比較もできるため、英語の発声レッスン等には、より一層効果を発揮する。

4. 図面の簡単な説明

第1図は、本発明実施例の録音機能付ヘッドホーンの回路構成図である。

1 …… 再生用スイッチ
2 …… スイッチ制御回路
3 …… 録音用スイッチ
4 …… スイッチ制御回路
5 …… 制御回路
6 …… アドレス回路
7 …… メモリ部
8 …… ADM復号化回路
9 …… 出力フィルタ
10 …… 出力アンプ
11 …… スピーカ
12 …… ADM符号化回路
13 …… 入力フィルタ
14 …… 入力アンプ
15 …… マイク
16 …… 入力端子

以　上

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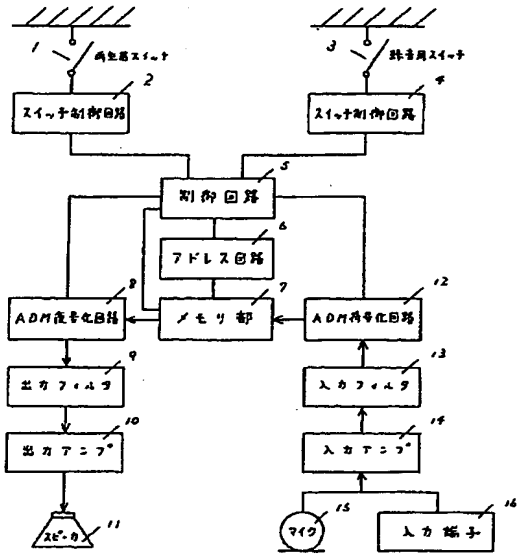
1
再生用スイッチ
2
スイッチ制御回路
3
録音用スイッチ
4
スイッチ制御回路
5
制御回路
6
アドレス回路
7
メモリ部
8
ADPM復号化回路
9
出力フィルタ
10
出力アンプ
11
スピーカ
12
ADPM符号化回路
13
入力フィルタ
14
入力アンプ
15
マイク
16
入力端子

第 1 図

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SPECIFICATION

1. Title of the Invention:

DISPLAY METHOD

2. Claim

(1) A display method characterized in that, when digital information is written to a semiconductor memory or digital information in the semiconductor memory is read, remaining time obtained by converting an access remaining amount of the semiconductor memory into time, completed time obtained by converting an access completed amount of the semiconductor memory into time, or both of the times are computed based on address information such as a current address and a last address of the semiconductor memory and access rate information of the semiconductor memory and display based on the remaining time, display based on the completed time, or display based on both of the times is

performed.

3. Detailed Description of the Invention

The present invention relates to a display method for displaying the access remaining amount of a semiconductor memory used for a storage device that stores record audio through digital conversion and that outputs playback audio through analog conversion of the stored digital information, the access completed amount of the semiconductor memory, or both of the amounts. An object of the present invention is to convert the access remaining amount, the access completed amount, or both of the amounts into time and display the time.

Conventionally, when an audio-signal storage device that uses a magnetic tape, such as a cassette tape or open reel tape, as a storage medium performs recording, playback, fast-forward, or the like, a change in the amount of tape at one side of the reel and the amount of tape at the other side of the reel can generally be viewed with eyes. Thus, it is possible to easily know the remaining time or the completed time of recording, playback, fast-forward, or the like. However, when the recording, playback, fast-forward, or the like is started from a half-way state, it is difficult to know the reaming time or the like from the half-way state.

On the other hand, some storage devices that convert

audio and music into digital information and store the information and that convert stored digital information into analog signal and output playback audio and playback sound use, as storage media, semiconductor memories for writing and reading digital information. For example, when recording, playback, fast-forward, and checking are performed by accessing such a semiconductor memory, it is impossible to view the access state of the semiconductor memory with eyes, thus making it difficult to known the remaining time and the completed time of the recording, playback, fast-forward, checking, or the like.

Although it is possible to know the capacity of the semiconductor memory by estimation based on the description on the package of a semiconductor memory or the actual use of the semiconductor memory, it is impossible to know the reaming time and the completed time from the capacity of the semiconductor memory. This is because time required for performing writing to or reading from the semiconductor memory varies depending on the access-completed time and access method of the semiconductor memory.

A cassette system that allows the attachment and detachment of the semiconductor memory and a fixed-type system that does not allow the attachment and detachment of the semiconductor memory are available for the storage devices.

With attention being paid to the above-described points, the present invention has been made by paying attention to the fact that time required for performing writing to and reading from the semiconductor memory is generally determined based on the capacity and the access time of the semiconductor memory. The present invention provides a display method characterized in that, when digital information is written to a semiconductor memory or digital information in the semiconductor memory is read, remaining time obtained by converting an access remaining amount of the semiconductor memory into time, completed time obtained by converting an access completed amount of the semiconductor memory into time, or both of the times are computed based on address information such as a current address and a last address of the semiconductor memory and access rate information of the semiconductor memory and display based on the remaining time, display based on the completed time, or display based on both of the times is performed.

Thus, when performing recording, playback, fast-forward, checking, or the like is performed on a storage device using a semiconductor memory, it is possible to know the remaining time of recording, playback, fast-forward, checking, or the like, the completed time thereof, or both of the times, based on the display of the access remaining time, access-

completed time, or both of the times. In particular, the present invention can provide a display method that is significantly effective for a storage device that stores audio, music, and so on by using a semiconductor memory.

Next, a display method of the present invention will be described in conjunction with a figure in which a first embodiment thereof is shown.

In the figure, (1) indicates a microphone for outputting an audio signal for recording, and (2) indicates a converter for performing digital conversion and analog conversion. The converter converts the audio signal from the microphone (1) and outputs digital audio information. (3) indicates a semiconductor memory in which the digital audio information from the converter (2) is written through a data bus (4). The semiconductor memory has a capacity of, for example, 128 kilobits, and digital audio information read from the memory (3) is input to the converter (2) through the data bus (4) and is converted by the converter (2) into an analog signal. (5) indicates a speaker to which a playback audio signal generated through the analog conversion by the converter (2) is input. Playback audio and playback sound are output from the speaker (5).

Additionally, (6) indicates a counter for outputting an address signal for accessing the semiconductor memory (3). The address signal from the counter (6) is input to the

semiconductor memory (3) through an address bus (7). (8) indicates a clock generator for outputting a clock signal for forming the address signal and (9) indicates a switch, which is provided between the counter (6) and the clock generator (8) and closes the path during recording, playback, fast-forward, and checking to send the clock signal to the counter (6). (10) indicates an address input unit implemented with a decimal keyboard. When accessing the semiconductor memory (3) is started from a desired halfway address in the memory (3), the address input unit initially forms an address signal, corresponding to the desired half-way address, and outputs the address signal to the counter (6), thereby initializing the counter (6).

Additionally, (11a), (11b), ... indicate multiple capacity-setting switches that are selectively operated in accordance with the capacity of the semiconductor memory (3), and (12a), (12b), ... indicate multiple rate-setting switches for setting an access rate for the semiconductor memory (3). (13) indicates a processing circuit to which the address signal is input through the address bus (7) and switch signals from the switches (11a), (11b), ..., (12a), (12b), ... are input. The processing circuit outputs clock control signals, which correspond to key signals of the rate-setting switches (12a), (12b), ..., to the clock generator (8) to control the frequency of the clock signal,

thereby controlling the output timing of the address signal from the counter (6). The processing circuit also computes and outputs remaining time, obtained by converting the access remaining amount of the semiconductor memory (3) into time; completed time, obtained by converting the access completed amount of the semiconductor memory (3) into time; or both of the times. (14) indicates a time display section to which a display signal from the processing circuit (13) is input. The time display section displays the above-described remaining time, the completed time, or both of the times.

For example, a parallel/serial converter circuit for digital audio information written to the semiconductor memory (3) and digital audio information read from the semiconductor memory (3) is omitted.

The semiconductor memory (3) is attached to a storage device. In accordance with key signals of the capacity setting switches (11a), (11b), ... corresponding to the capacity of the semiconductor memory (3), a last address based on the capacity of the semiconductor memory (3) is input to the processing circuit (13). Also, in accordance with the key signals of the predetermined rate-setting switches (12a), (12b), ..., access rate information for performing writing to and reading from the semiconductor memory (3), for example, access rate information of 2400

bits/second, is input to the processing circuit (13).

Based on the key signals of the rate-setting switches (12a), (12b), ..., the frequency of the clock signal to be output from the clock generator (8) to the counter (6) is set.

With an access rate set to 2400 bits/second, when the capacity of the semiconductor memory (3) is 128 kilobits, time required for completing writing to or reading from the semiconductor (3) is about 53 seconds.

Next, when a mode switch (not shown) for recording, playback, fast-forward, checking, and so on is operated to perform recording, playback, fast-forward, checking, or the like, the semiconductor memory (3) is accessed in accordance with the address signal that is output from the counter (6) to the semiconductor memory (3) through the address bus (7) and the address signal from the address bus (7) is input to the processing circuit (13).

Further, the processing circuit (13) compute remaining time, which is time converted from the access remaining amount of the semiconductor memory (3), by subtracting the current address from the last address and dividing the subtraction result by rate information; computes access completed time, which is time converted from the access completed amount of the semiconductor memory (3), by subtracting the current address by rate information; or

computes both of the times.

In addition, in accordance with the display signal from the processing circuit (13), the computed remaining time, completed time, or both of the times are displayed on the time display section (14).

Based on the time displayed on the time display section (14), it is possible to know the remaining time, the completed time, or both of the times for recording, playback, fast-forward, checking or the like.

In the embodiment described above, although the capacity-setting switches (11a), (11b), ... for detachably attaching the semiconductor memory having a different capacity to the storage device is provided, they can be eliminated in the case of a fixed-type storage device. Naturally, without the provision of the capacity-setting switches (11a), (11b), ..., the last address of the semiconductor memory (3), the last address being based on the capacity of the semiconductor memory (3), can also be automatically input to the processing circuit (13).

In addition, when the access rate of the semiconductor memory (3) is not changed, the rate-setting switches (12), (12b), ... can be eliminated.

4. Brief Description of the Drawing

The figure is a block diagram according to a first embodiment of a display method of the present invention.

(3) ... semiconductor memory; (6) ... counter; (7) ... address bus; (11a), (11b) ... capacity-setting switches; (12a), (12b) ... rate-setting switches; (13) ... processing circuit; (14) ... time display section